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Notice of Allowability	Application No.	Applicant(s)
	10/707,205	PILEGGI ET AL.
	Examiner	Art Unit
	Cynthia Britt	2117
The MAILING DATE of this communication apply All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.313	(OR REMAINS) CLOSED i) or other appropriate comm (IGHTS. This application is	n this application. If not included unication will be mailed in due course. THIS
1. \boxtimes This communication is responsive to <u>6/6/07</u> .		
2. X The allowed claim(s) is/are <u>1-22,24-42,52,54-64 and 66-7</u>	<u>o</u> .	
 3. Acknowledgment is made of a claim for foreign priority uner a) All b) Some* c) None of the: 1. Certified copies of the priority documents have 2. Certified copies of the priority documents have 	e been received.	
Copies of the certified copies of the priority do		
International Bureau (PCT Rule 17.2(a)).	ocuments have been receive	ed in this national stage application from the
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDONN THIS THREE-MONTH PERIOD IS NOT EXTENDABLE. 4. A SUBSTITUTE OATH OR DECLARATION must be subm	MENT of this application. nitted. Note the attached EX	AMINER'S AMENDMENT or NOTICE OF
INFORMAL PATENT APPLICATION (PTO-152) which giv	es reason(s) why the oath o	or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") mu	st be submitted.	
(a) including changes required by the Notice of Draftspers		w (PTO-948) attached
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date	<u>.</u> .	
(b) including changes required by the attached Examiner Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR 1)		
each sheet. Replacement sheet(s) should be labeled as such in	the header according to 37 C	rne drawings in the front (not the back) of FR 1.121(d).
 DEPOSIT OF and/or INFORMATION about the depo attached Examiner's comment regarding REQUIREMENT 	osit of BIOLOGICAL MAT FOR THE DEPOSIT OF BI	ERIAL must be submitted. Note the OLOGICAL MATERIAL.
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of Ir	nformal Patent Application
2. Notice of Draftperson's Patent Drawing Review (PTO-948)		Summary (PTO-413), /Mail Date
Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date	7. 🛭 Examiner's	s Amendment/Comment
4. Examiner's Comment Regarding Requirement for Deposit of Biological Material	8. Examiner's	Statement of Reasons for Allowance
	9.	Cynthia Britt
•		PRIMARY EXAMINER

EXAMINER'S AMENDMENT

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An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

This application is in condition for allowance except for the presence of claims 43-51 directed to the group non-elected without traverse.

Accordingly, claims 43-51 have been cancelled.

Claims 23, 53, and 65 were previously cancelled.

Claims 1-22, 24-42, 52, 54-64, and 66-70 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references and those cited on Form 892 are considered pertinent to the claimed invention.

"Testability and Yield of MMICs" by Allen, B.R. This paper appears in: Antennas and Propagation Society International Symposium, 1992 Digest. Held in Conjunction with: URSI Radio Science Meeting and Nuclear EMP Meeting., IEEE Publication Date: 18-25 Jul 1992 On page(s): 1263 vol.3 ISBN: 0-7803-0730-5 INSPEC Accession

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This paper teaches an approach to MMIC (monolithic microwave integrated circuit) yield measurement involving on-wafer functional testing was discussed. On-wafer RF testing, combined with minimum DC testing, provides the necessary testing of individual chips with minimum costs. The on-wafer tests used to screen MMICs for yield current include measurements of output power, complex gain, return loss, noise, and spurious output. To provide effective on-wafer screening of MMICs, testability must be included as part of the design. The design issues that influence on-wafer testability include pad placement, stability, number of connections, and thermal resistance. The testing required to identify good die may range from full functional testing of every specification to simple DC screening. The required level of testing is usually related to the performance requirements of the chip and the design margins.

"Measurement Challenges for on-wafer RF-SOC test" by Wai Yuen Lau This paper appears in: 27th Annual IEEE/SEMI International Electronics Manufacturing Technology Symposium, 2002. Publication Date: 2002 On page(s): 353- 359 ISBN: 0-7803-7301-4 INSPEC Accession Number: 7492523

This paper teaches that with the wireless industry pushing towards higher levels of integration, with more system-in-a-package (SIP) and multi-chip module (MCM) technology, known-good-die testing of RF-SOC devices has emerged as the next test challenge. These devices have higher packaging costs compared to the traditional single die integrated circuits (ICs), and potential lower yields, since multiple dice are used. As a result, the cost to perform comprehensive on-wafer testing is outweighed by

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the cost to scrap the devices during the final package test. In addition, some IC manufacturers are selling bare die to be used in the SIP or MCM of another manufacturer. On-wafer test is then required to ensure that good product is shipped. This paper will use a Bluetooth radio modem chip as an example to discuss the measurement challenges and considerations for known-good die testing of a RF-SOC device. With this example, the difficulty of testing RF functionality on-wafer will be compounded by the need to source and measure RF and digital signals simultaneously, creating signal integrity issues. This paper explores the challenges of laying out the printed circuit board for the device under test (DUT), including setup of the wafer probe card and assembly. Factors taken into account when selecting a probe station, RF wafer probe card, and ATE test system will then be discussed. This paper concludes with a discussion of on-wafer calibration, including challenges and solutions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt Primary Examiner Art Unit 2117

CYNTHIA BRITT
PRIMARY EXAMINER